IN THE CLAIMS:

Please amend claims 1-16 as indicated below.

Please add new claims 19-27 as indicated below.

1. (Currently Amended) A memory controller, comprising:

a plurality of tag units, each tag unit including an array of tag address storage locations, the plurality of tag units to perform tag look-up operations in response a memory access request;

a memory module decode unit, the memory module decode unit to perform decode operations to determine which one of a plurality of memory modules is being accessed by the memory access request substantially concurrently with respect to ~~in parallel with~~ the tag look-up operations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations and the memory module decode unit, the command sequencer and serializer unit to serialize commands and address information and sequentially transmit, over a serial link of a memory bus coupling the memory control with a plurality of memory modules, to a memory module to access a data cache located on the memory module that is specified by the memory module decode unit as a result of the decode operations, if the lookup operations indicate that at least one of the tag addresses matches a memory address of the memory access request ~~control a plurality of data caches, each data cache located on one of a plurality of memory modules, the memory modules coupled to the memory controller via a memory bus~~.

2. (Currently Amended) The ~~apparatus~~ memory controller of claim 1, wherein each of the plurality of tag units is corresponding to one of the plurality of memory modules.

3. (Currently Amended) The ~~apparatus~~ memory controller of claim 2, wherein the tag look-up operations are to provide cache hit information.

4. (Currently Amended) The ~~apparatus~~ memory controller of claim 3, wherein the tag look-up operations are to provide cache line modified information.

5. (Currently Amended) The ~~apparatus~~ memory controller of claim 4, wherein each of the arrays of tag address storage locations is organized into a plurality of cache ways, each cache way representing how cache lines of a cache memory of a memory module are mapped to system memory addresses.

6. (Currently Amended) The ~~apparatus~~ memory controller of claim 5, wherein the tag look-up operations are to provide way information implicating how the cache lines being address in a current transaction is mapped to the system memory addresses.

7. (Currently Amended) The ~~apparatus~~ memory controller of claim 6, wherein each of the arrays of tag address storage locations is organized into 4 ways

8. (Currently Amended) The ~~apparatus~~ memory controller of claim 1, wherein the command sequencer and serializer unit is to control the plurality of data caches located on

the plurality of memory modules by delivering commands over the memory bus, the memory bus including a plurality of command and address lines.

9. (Currently Amended) The ~~apparatus~~ memory controller of claim 8, wherein the plurality of command and address lines are part of a point-to-point interconnect that transmits signals over one or more serial links between the memory controller and the memory modules.

10. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

a plurality of tag units, each tag unit including an array of tag address storage locations, the plurality of tag units to perform tag look-up operations in response to a memory access request,

a memory module decode unit, the memory module decode unit to perform decode operations to determine which one of a plurality of memory modules is being accessed by the memory access request substantially concurrently with respect to ~~in parallel with~~ the tag look-up operations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations and the memory module decode unit; and

a plurality of memory modules coupled to the memory controller via a memory bus, each of the plurality of memory modules including

a memory device, and

a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller,

wherein the command sequencer and serializer unit is to access, over the memory bus, a data cache located on one of the memory module that is specified by the memory module decode unit as a result of the decode operations, if the lookup operations indicate that at least one of the tag addresses matches a memory address of the memory access request.

11. (Currently Amended) The system of claim 10, wherein the memory bus ~~being~~ is a point-to-point interconnect to couple the memory controller to the memory modules.

12. (Currently Amended) The system of claim 11, wherein the arrays of tag address storage locations and the data caches are organized into a plurality of ways.

13. (Currently Amended) The system of claim 12, wherein the tag look-up operations are to provide cache hit information.

14. (Currently Amended) The system of claim 13, wherein the tag look-up operations are to provide cache line modified information.

15. (Currently Amended) The system of claim 14, wherein the tag look-up operations are to provide way information.

16. (Currently Amended) A method, comprising:

receiving a read request at a memory controller;

performing a tag look-up by a plurality of tag units within the memory controller to determine whether there is a cache hit for the read request, each tag unit including an array of tag address storage locations;

determining by a memory module decode unit which of a plurality of memory modules is addressed by the read request, wherein performing a tag look-up and determining which of a plurality of memory modules is addressed by the read request occur in parallel; and

fetching by a command sequencer and serializer unit coupled to the tag units and the memory module decode unit a line of cache data from a data cache located on one of the plurality of memory modules if the tag look-up indicates a cache hit, the memory modules separate from the memory controller and coupled to the memory controller via a memory bus.

17. (Original) The method of claim 16, wherein performing a tag look-up includes providing way information.

18. (Original) The method of claim 17, wherein performing a tag look-up operation includes providing cache line modified information.

19. (New) The memory controller of claim 1, further comprising a memory bank and address decode unit coupled to the command sequencer and serializer unit and the plurality of tag units to determine a row address and a column address of a bank of memory device that a current memory transaction addresses.

20. (New) The memory controller of claim 19, wherein the command sequencer and serializer accesses a memory location at the row and column addresses of a bank of memory device determined by the memory bank and address decode unit within a memory module determined by the memory module decode unit.

21. (New) The memory controller of claim 1, further comprising a multiplexer coupled to the memory decode unit, the plurality of tag units, and the command sequencer and serializer unit, the multiplexer multiplexing a plurality of way signals, hit signals, and modified signals generated from the plurality of tag units to a single set of a way signal, a hit signal, and a modified signal based on a decode operation performed by the memory module decode unit, the single set of the way signal, hit signal, and modified signal being transmitted from the multiplexer to the command sequencer and serializer unit.

22. (New) The memory controller of claim 9, wherein the point-to-point interconnect comprises 8 differential pairs, 9 pairs for data, and 9 pairs for address and command.

23. (New) The memory controller of claim 9, wherein the point-to-point interconnect comprises 27 differential pairs, 18 pairs for data, and 9 pairs for address and command.

24. (New) The memory controller of claim 1, wherein each of the tag units comprises one or more tag way units containing a respective array of tag addresses, each of the tag way unit corresponding to a respective way of an associative cache set.

25. (New) The memory controller of claim 24, wherein each tag way unit generates tag data containing cache lines associated with an index for the respective tag way unit using a first portion of address lines an index.

26. (New) The memory controller of claim 25, wherein each tag way unit further comprises a comparator coupled to each tag way unit and the address lines to compare the received tag data with a second portion of the address lines in order to determine whether there is a tag match indicating as a hit.

27. (New) The memory controller of claim 26, wherein each tag way unit further generates a valid signal indicating which cache lines associated with a tag address are valid when the cache is configured as a segmented cache.